REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants have amended claim 33 to recite that all of the at least one external connection terminal are provided only inside of the wire bonding terminal. Claim 36 has been amended to correct a typographical error.

Moreover, Applicants have added new claims 38-40 to the application. Claim 38, dependent on claim 33, recites that the external connection terminal (recited in claim 33) is one of a plurality of external connection terminals, exposed on a surface of the insulating supporting member on an opposite side to which the semiconductor device is mounted, with all of the plurality of external connection terminals being located only inside of the wire bonding terminal. Claims 39 and 40, dependent respectively on claims 38 and 33, recite that the wire bonding terminal (recited in claim 33) is one of a plurality of wire bonding terminals of the substrate, with the external connection terminal(s) being positioned only within the plurality of wire bonding terminals.

Applicants respectfully submit that all of the claims presented for consideration by the Examiner patentably distinguish over the teachings of the references applied by the Examiner in the Office Action mailed November 2, 2004, that is, the teachings of the U.S. Patents to Pennisi et al, No. 5,313,365, and to Dougherty, Jr. et al, No. 4,602,271, and Japanese Patent Document No. 59-208756 (Katsuhiko), under the provisions of 35 U.S.C. §102 and 35 U.S.C. §103.

It is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a substrate for mounting

semiconductor devices thereon, as in the present claims, including, inter alia, wherein the substrate has a semiconductor device mounting region and a resin-sealing semiconductor package region outside of this semiconductor device mounting region, and wherein the wire bonding terminals are provided in the semiconductor package region and the external connection terminals are provided only within the semiconductor device mounting region. See claim 32.

In addition, it is respectfully submitted that these applied references would have neither taught nor would have suggested such a substrate for mounting semiconductor devices thereon as in the present claims, including, inter alia, wiring which includes a wire bonding terminal and at least one external connection terminal, and with all of the at least one external connection terminal being provided only inside of the wire bonding terminal. See claim 33.

Moreover, it is respectfully submitted that these references as applied by the Examiner would have neither disclosed nor would have suggested such a substrate as in the present claims, having features as discussed previously in connection with claim 33, and, moreover, wherein the substrate has a plurality of external connection terminals, exposed on the surface of the insulating supporting member on an opposite side thereof to which the semiconductor device is mounted, and wherein all of these plurality of external connection terminals are located only inside of the wire bonding terminal. See claim 38.

In addition, these applied references would have neither taught nor would have suggested such substrate as in the present claims, with a plurality of wire bonding terminals, and with the external connection terminal(s) only within the plurality of wire bonding terminals. See claims 39 and 40.

Furthermore, it is respectfully submitted that the teachings of these applied references would have neither disclosed nor would have suggested such a substrate for mounting semiconductor devices thereon, or a semiconductor package produced using such substrate, the substrate having features as discussed previously in connection with claim 33, and, moreover, wherein the substrate includes a plurality of wiring patterns comprised of a plurality of the wirings arranged in rows and columns (see claim 34); and/or wherein the wire/bonding terminal includes a nickel layer and a gold plate layer on its surface (see claim 35); and/or wherein the external connection terminal is one of a plurality of external connection terminals, exposed on a surface of the insulating supporting member on an opposite to which the semiconductor device is mounted, with the external connection terminals being arranged in a grid pattern at positions corresponding to a semiconductor device mounting region and a semiconductor package region of the substrate (see claim 36); and/or wherein the substrate of claim 33 is used to mount a semiconductor device on each of the plural semiconductor device mounting regions by employing a die-bonding material and electrically connecting a semiconductor device with the wire-bonding terminals by wire-bonding, sealing the semiconductor device region including a semiconductor device with a sealing resin connected in one-piece forming solder bumps on the external connection terminals and cutting the substrate and sealing resin in one operation to be separated into the individual semiconductor package, in producing the recited semiconductor package (see claim 37).

According to the presently claimed invention, the substrate used provides a "fan-in" structure (namely, the wire-bonding terminals are provided in the packaging region and the external connection terminals are provided, e.g., in the semiconductor

mounting region located inward of the packaging region. By providing the external connection terminals only in the semiconductor device mounting region (namely, only inward of the wire-bonding terminals), chip-size packaging can be achieved.

In addition, using the substrate of the present invention, the semiconductor device and a substrate can be connected by a wire-bonding, so that a large number of small-sized semiconductor packages can be produced in a simple process, at a very low cost.

Pennisi et al, discloses electronic packages for semiconductor devices and integrated circuits, in particular encapsulation of semiconductors directly attached to a circuit substrate. According to the encapsulated electronic package of Pennisi et al, a printed circuit board is provided with a metal circuit pattern on one side. One or more semiconductor devices are attached to the printed circuit board with an adhesive, and covered by a glob top encapsulant. The glob top encapsulant also covers portions of the printed circuit board surface. The resin used to make the printed circuit board, adhesive and the encapsulant are an organosilicon polymer comprised substantially of alternating polycyclic hydrocarbon residues and cyclic polysiloxane or siloxysilane residues linked through carbon-silicon bonds. See column 2, lines 22-36. Note also column 3, lines 5-8 and 16-18.

As can be seen in, for example, Fig. 1 of Pennisi et al, clearly the external connection terminal (which are not numbered in Fig. 1) are provided outside the semiconductor device mounting regions, and are also provided outside of the wire bonding terminals 12. In any event, clearly the drawing figures of Pennisi et al, are schematic and not in engineering drawings to scale, and it is respectfully submitted that the teachings of this reference do not disclose, nor would have suggested,

structure wherein the external connection terminals are provided only within the semiconductor device mounting region (see claim 32); and/or wherein all of the external connection terminals are provided only inside of the wire bonding terminal (see claim 33; note also claim 38).

It is respectfully submitted that addition teachings of the secondarily applied references would not have rectified the deficiencies of Pennisi et al, such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Dougherty et al, discloses a package for semiconductor chips, wherein a substrate is provided with a repeating pattern of conductor ends, with each pattern defining sites to permit the reception of a variety of different chips. The substrate of the described package is provided having a chip mounting surface, and is structured with conductors having opposite ends terminating at the mounting surface with intermediate portions connecting the ends of the conductors, the ends of the conductors being arranged in repeating patterns longitudinally along the substrate separated by orthogonal strips on the surface which are free of conductor ends to allow for dense surface wiring. The immediate portions of some conductors connected ends within a pattern and of some conductors connect ends in adjacent patterns. The conductor ends in each pattern are positioned to delineate a plurality of chip mounting sites having sufficient spacing between the conductor ends to permit the positioning of chip mounting means which may be electrically connected to the ends of the conductors by surface metallization. The substrate in Dougherty et al uses subsurface conductors to provide basic interconnection within each pattern and between adjacent patterns, and surface wiring for unique chip mounting and

wiring. See from column 1, line 51 to column 2, line 9. Note also column 2, lines 38-45; and column 3, lines 4-6.

It is respectfully submitted that Dougherty et al, discloses multiple levels of wiring in a vertical direction. It is respectfully submitted that Dougherty et al, either alone or in combination with the teachings of Pennisi et al, would have neither disclosed nor would have suggested such substrate or such package produced using such substrate, as in the present claims, including, inter alia, wherein the external connection terminals are provided only within the semiconductor device mounting region, and/or wherein all of the external connection terminals are provided only inside of the wire bonding terminal.

The contention by the Examiner on page 4 of the Office Action mailed November 2, 2004, that Pennisi et al discloses a substrate wherein the external connection terminals are provided only within the semiconductor device mounting region, the Examiner referring to Figs. 1 and 2 of Pennisi et al, is respectfully traversed. As stated previously, it is respectfully submitted that the drawing figures of Pennisi et al, are schematic drawing figures, not engineering scale drawings, and can not be used for measuring purposes. Furthermore, clearly the (unnumbered) external wiring terminals in Fig. 1 of Pennisi et al include terminals falling outside the wire bonding terminals 12, and it is respectfully submitted that Pennisi et al would have taught away from the presently claimed invention, including wherein the external connection terminals are provided only within the semiconductor device mounting region. Moreover, looking at the (unnumbered) external connection terminals in Fig. 1 of Pennisi et al, it is respectfully submitted that these external connection terminals are at best at same locations (vertically) as wire bonding

terminals 12, and it is respectfully submitted that the disclosure of Pennisi et al would have taught away from structure as in the present claims, including wherein all of the external connection terminals are provided only inside of the wire bonding terminal (see claim 33).

Katsuhiko discloses a semiconductor device package excellent in heat radiation and suitable for automated manufacturing. This patent document discloses a gold plating 12 of one 1μm thickness, nickel plating 13 of 1μm thickness and gold plating 14 of 3μm being laminated on an iron substrate 11 of 35 μm thickness, with a semiconductor chip 15 mounted 16 on a portion 11g and connected 19 to external electrodes 17, 18 on the portions 11h, 11i. Transfer-molding with epoxy resin 20 is carried out so as to make thickness t (see Fig. 2C) = 1mm. The iron substrate is removed to complete a leadless type package 21. Note particularly, for example, Figs. 2D, 4B and 5C of this applied Japanese Patent Application.

As can particularly be seen in Figs. 2D, 4B and 5C of Katsuhiko, the exposed external wiring terminals extend below the wire bonding terminals, and are clearly outside the semiconductor device mounting region. It is respectfully submitted that the teachings of Katsuhiko, in combination with the teachings of the other applied references, would have neither disclosed nor would have suggested such substrate or such semiconductor package as in the present claims, wherein, inter alia, the external connection terminals are provided only within the semiconductor device mounting region, and/or wherein the external connection terminals are provided only inside of the wire bonding terminals, and advantages of this structure as discussed previously; and/or the other features of the present invention as discussed previously, and advantages thereof.

In view of the foregoing comments and amendments, reconsideration and allowance of all claims presently pending in the above-identified application are respectfully requested.

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Respectfully submitted,

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